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APPLICATION FOR LETTERS PATENT

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Thin Film Transistors And Methods Of Forming Thin Film Transistors

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PATENT RIGHTS STATEMENT

This invention was made with Government support under Contract No. MDA972-92-C-0054 awarded by Advanced Research Projects Agency (ARPA). The Government has certain rights in this invention.

TECHNICAL FIELD

This invention relates specifically to thin film transistor technology.

BACKGROUND OF THE INVENTION

As circuit density continues to increase, there is a corresponding drive to produce smaller and smaller field effect transistors. Field effect transistors have typically been formed by providing active areas within a bulk substrate material or within a complementary conductivity type well formed within a bulk substrate. One additional technique finding greater application in achieving reduced transistor size is to form field effect transistors with thin films, which is commonly referred to as "thin film transistor" (TFT) technology. These transistors are formed using thin layers which constitute all or a part of the resultant source and drain regions, as opposed to providing both regions within a bulk semiconductor substrate.

Specifically, typical prior art TFT's are formed from a thin film of semiconductive material (typically polysilicon). A central channel

region of the thin film is masked by a separate layer, while opposing adjacent source/drain regions are doped with an appropriate p or n type conductivity enhancing impurity. A gate insulator and gate are provided either above or below the thin film channel region, thus providing a field effect transistor having active and channel regions formed within a thin film as opposed to a bulk substrate.

It would be desirable to improve upon methods of forming thin film transistors and in improving thin film transistor constructions.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is one example of a possible top view of Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 6 is a diagrammatic sectional view of an alternate embodiment wafer fragment in accordance with the invention.

Fig. 7 is a diagrammatic sectional view of yet another alternate embodiment wafer fragment at one processing step in accordance with the invention.

Fig. 8 is a view of the Fig. 7 wafer fragment at a processing step subsequent to that shown by Fig. 7.

Fig. 9 is a view of the Fig. 7 wafer fragment at a processing step subsequent to that shown by Fig. 8.

Fig. 10 is a view of the Fig. 7 wafer fragment at a processing step subsequent to that shown by Fig. 9.

Fig. 11 is a view of the Fig. 7 wafer fragment at a processing step subsequent to that shown by Fig. 10.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In accordance with one aspect of the invention, a method of forming a thin film transistor over a substrate comprises the following steps:

providing a layer of semiconductive material from which a channel region and at least one of a source region or a drain region of a thin film transistor are to be formed; and

conductively doping the at least one of the source region or the drain region of the semiconductive material layer while preventing conductivity doping of the channel region of the semiconductive material layer, such doping being conducted without any masking of the channel region by any separate masking layer.

In accordance with another aspect of the invention, a method of forming a thin film transistor comprises the following steps:

providing a substrate having a node to which electrical connection is to be made;

providing a first electrically insulative dielectric layer over the substrate;

providing an electrically conductive gate layer over the first dielectric layer;

providing a second electrically insulative dielectric layer over the electrically conductive gate layer;

providing a contact opening through the second dielectric layer, the electrically conductive gate layer and the first dielectric layer; the contact opening defining projecting sidewalls;

providing a gate dielectric layer within the contact opening laterally inward of the contact opening sidewalls;

providing a layer of semiconductive material over the second dielectric layer and within the contact opening against the gate dielectric layer and in electrical communication with the node; the semiconductive material within the contact opening defining an elongated and outwardly

extending channel region the electrical conductance of which can be modulated by means of the adjacent electrically conductive gate and gate dielectric layers; and

conductively doping the semiconductive material layer lying outwardly of the contact opening to form one of a source region or a drain region of a thin film transistor.

In accordance with still another aspect of the invention, a thin film transistor comprises:

a thin film transistor layer having a source region, a channel region and a drain region; the thin film channel region comprising an annulus; and

a gate in proximity to the thin film channel annulus, the gate comprising an annulus which surrounds the thin film channel annulus.

These and other aspects of the invention will be more readily appreciated from the following description with proceeds with reference to the accompanying drawings.

Referring to Fig. 1, a semiconductor wafer fragment in process is indicated generally with reference numeral 10. Such comprises a bulk substrate 12 of lightly doped p or n type monocrystalline silicon, having a diffusion region 13 provided therein. A first electrically insulative dielectric layer 14 (typical SiO_2) is provided over bulk substrate 12. An example and preferred thickness range for layer 12 is from 50 Angstroms to 2000 Angstroms, with 100 Angstroms being more preferred. An electrically conductive layer 16 is provided over first

dielectric layer 14. Layer 16 will ultimately comprise the conductive gate of the thin film transistor, and preferably comprises a heavily doped (greater than 1 x 10^{20} ion/cm^3) layer of polysilicon. An example and preferred thickness range is from 3000 Angstroms to 10,000 Angstroms, with 8000 Angstroms being more preferred. A second electrically insulative dielectric layer 18 is provided over electrically conductive gate layer 16. Such can be considered as a base layer over which a thin film transistor layer will be provided. An example and preferred material is SiO_2 deposited to a thickness range of from 300 Angstroms to 3000 Angstroms, with 1000 Angstroms being more preferred.

Referring to Fig. 2, a contact opening 20 is provided through second dielectric layer 18, electrically conductive gate layer 16, and first dielectric layer 14 to outwardly expose diffusion region 13. Alternately, diffusion region 13 could be provided after forming contact opening 20. One method of doing this is by using ion implantation through contact opening 20, thereby making diffusion regions 13 self-aligned to contact opening 20. Contact opening 20 defines projecting sidewalls 22 which in the preferred embodiment are provided to be substantially perpendicular relative to the expanse of bulk substrate 12. A dielectric layer 24, which will serve as gate dielectric layer, is deposited over second dielectric layer 18 and within contact opening 20 to a thickness which less than completely fills contact opening 20. An example diameter for contact opening 20 is 3500 Angstroms, with an example

layer 24 being SiO_2 deposited to a thickness of 200 Angstroms in such instance.

Referring to Fig. 3, gate dielectric layer 24 is anisotropically etched to define a resultant gate dielectric layer 26 within contact opening 20 laterally inward of sidewalls 22. When anisotropically etching gate dielectric layer 24, some of second dielectric layer 18 is removed during a desired overetch. If layer 18 is 1000 Angstroms thick and layer 24 is 200 Angstroms thick, a preferred over-etch would be 200 Angstroms, reducing 18 to 800 Angstroms. In the illustrated and preferred embodiment, such gate dielectric layer takes on the shape or appearance of conventional insulative sidewall spacers, and in the depicted embodiment is in the form or shape of a longitudinally elongated annulus. Thus, electrically conductive gate layer 16 also is comprised of an annulus which surrounds contact opening 20.

Fig. 4 illustrates one example of a possible patterned top construction of Fig. 3. Such illustrates gate dielectric annulus 26 encircling within contact opening 20. Electrically conductive gate layer 16 has been patterned to comprise a ring portion and an extension 27. Regardless, the bulk mass of layer 16 constitutes an annulus which encircles contact opening 20. The above described process provides but one example of a manner in which a gate dielectric layer is provided within contact opening 20.

Referring to Fig. 5, a layer 30 of semiconductive material is provided over second dielectric layer 18 and within contact opening 20

against gate dielectric layer 26, and in electrical communication with diffusion region 13. In this particular described embodiment, layer 30 is provided to completely fill the remaining open portion of contact opening 20. Semiconductive material layer 30 constitutes a layer from which a channel region and at least one of a source region or a drain region of a thin film transistor are to be formed. The semiconductive material of layer 30 within contact opening 20 defines an elongated and outwardly extending channel region 31 the electrical conductance of which can be modulated by means of the adjacent electrically conductive gate and gate dielectric layers 16 and 26, respectively.

Field effect transistor channel regions typically utilize some minimum conductivity doping, less than the doping concentrations of the source and drain, to provide desired conductance when modulated by the gate. Such can be provided in this example by *in situ* doping of layer 30 during its deposition. Alternately, an ion implant can be conducted with subsequent processing providing desired diffusion of the dopants.

The semiconductive material layer 30 is then conductively doped such that its portion lying outwardly of contact opening 20 forms one of a source or a drain region 32 of a thin film transistor. The doping results in an interface 34 being created relative to the outermost portions of layer 30 and that portion within channel region 31, such that portion 32 constitutes a highly doped electrically conductive region, while channel region 31 constitutes a semiconductive layer capable of

being rendered conductive by applying suitable voltage to gate layer 16. Note that advantageously in accordance with the preferred process, conductive doping of layer 30 is conducted using its thickness to effectively prevent conductivity doping of channel region 31, with such doping being conducted without other masking of the channel region by any separate masking layer. The effective thickness and doping conditions for the outer portion of layer 30 effectively can be utilized to prevent undesired conductivity enhancing doping of channel region 31.

In the above described embodiment, one of doped regions 32 of layer 30 or diffusion region 13 of bulk substrate 12 constitutes a source region of a thin film transistor, while the other of such constitutes a drain region. Region 31 constitutes a channel region, with gate layer 16 comprising an annulus which encircles thin film channel region 31. Both of channel region 31 and diffusion region 32 are elongated, with diffusion region 32 being oriented substantially perpendicular relative to channel region 31 and also substantially parallel with bulk substrate 14. Elongated channel region 31 and gate dielectric annulus 26 are perpendicularly oriented relative to bulk substrate 14.

If region 13 constitutes the drain region, then the thickness of oxide layer 14 defines the gate-drain offset dimension of the thin film transistor. As well known to those of skill in the art, a drain offset is a region used in thin film transistors to reduce off current caused by thermionic field emission in the channel region near the drain. If region 32 is the drain, then the thickness of layer 18 defines the offset

dimension. The thickness of gate polysilicon layer 16 defines the channel length of the thin film transistor.

An alternate embodiment is shown and described with reference to Fig. 6. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated by the suffix "a" or with different numerals. In the depicted embodiment of wafer fragment 10a, semiconductive material 30a is provided to only partially fill the remaining portion of contact opening 20. Such forms an annulus 33 within contact opening 20, with such annulus being utilized to comprise the channel region of the resultant thin film transistor.

Layer 30a can be doped in a single step to form diffusion regions 32a and 35, one of which constitutes a drain region and the other of which constitutes a source region of the resultant thin film transistor. Accordingly, channel annulus 33 is elongated and oriented substantially perpendicularly relative to bulk substrate 12 and diffusion regions 32a and 35. In this described embodiment, gate layer 16 comprises an annulus which surrounds thin film channel annulus 33. Again, the elongated and substantially vertical nature or orientation of channel region 33 prevents conductivity doping from occurring therein when regions 32a and 35 are doped by a highly directional perpendicular ion implantation doping. In this embodiment, diffusion region 13 constitutes a node to which electrical connection of a thin film transistor is to be made, while in the first embodiment example region 13 comprised an inherent part of the thin film transistor.

Diffusion region 13 might alternately be provided by out-diffusion of dopant material from region 35 from subsequent heating steps.

Desired minimum doping for the channel region of Fig. 6 can be provided by *in situ* doping or by ion implanting, such as angled implanting.

Yet another alternate preferred embodiment is described with reference to Figs. 7-11. Like numerals from the first described embodiment have been utilized where appropriate, with differences being indicated with the suffix "b" or with different numerals. Referring first to Fig. 7, second electrically insulative dielectric layer 18 is provided with an initial contact opening 50 therethrough to electrically conductive gate layer 16. A preliminary electrically insulative layer 52 is provided over second dielectric layer 18 and to within initial contact opening 50, with such layer less than completely filling contact opening 50.

Referring to Fig. 8, preliminary electrically insulative layer 52 is anisotropically etched to define an insulative annulus spacer 54 within initial contact opening 50. Such facilitates or enables producing a contact opening inwardly of the spacers which is less than the minimum photolithographic feature size which can be useable to produce the smallest possible initial contact opening 50. For example, where a minimum available photolithographic width for contact opening 50 were 0.32 micron, the resultant width of the opening after spacer etch can be reduced to 0.1 micron. As examples, if layer 18 is 1500 Angstroms thick and opening 50 is 3200 Angstroms in diameter, layer 52 is

preferably provided to a thickness of from 500 Angstroms to 1200 Angstroms, with 1000 Angstroms being most preferred. An anisotropic etch of a 1000 Angstrom thick layer 52 will preferably be conducted as an over-etch of 300 Angstroms, leaving layer 18 1200 Angstroms thick.

Referring to Fig. 9, a secondary contact 56 is etched through electrically conductive gate layer 16 and first dielectric layer 14. During such etching, insulative annulus spacer 54 and second dielectric layer 18 are used as an etching mask. Diffusion regions 13b is provided as shown.

Referring to Fig. 10, a secondary electrically insulative layer 58 is provided over second dielectric layer 18 and insulative annulus spacer 54 to within secondary contact opening 56, with such layer being provided to less than completely fill secondary contact opening 56.

Referring to Fig. 11, secondary electrically insulative layer 58 has been anisotropically etched to define a gate dielectric layer annulus 26b within secondary contact opening 56. A subsequent semiconductive layer 30b is provided and doped as shown to provide diffusion region 32b, and to provide channel region 31b. An example thickness for layer 58 is 200 Angstroms. Anisotropic etching of such a layer preferably includes a 200 Angstrom over-etch, resulting in a final preferred thickness of layer 18 of 1000 Angstroms.

The above described embodiments utilizing an annulus gate essentially enables provision of a channel region which is gated about

all sides, thus enabling provision of smaller field effect transistors. Such results in a reduced consumption of substrate area, with such example thin film transistors enabling the required area to be that of the contact and the associated anisotropic spacer-like constructions. Conventional horizontal thin film transistors require additional area for the channel, source and drain regions. Such also provides for improved thin film transistor characteristics, due to gating of the channel region on all sides which provides greater controllable on/off currents.

The above described method and embodiment further reduce overall mask count in semiconductor processing. Since in the preferred embodiment the channel region is substantially vertical, masks are not required to protect the desired channel from the thin film transistor source and drain implants. Depending on implementation, the channel region may even be completely sealed from the surface providing even greater protection, thus eliminating at least two masks.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.